REMARKS

Claims 1-20 and 23-24, as amended, and new claims 25-26 appear in this application for the Examiner's review and consideration. The new claims are fully supported by the specification at paragraphs [0048] and [0157] so that there is no new matter being introduced. Also, claims 16 and 18 are directed to preferred embodiments and have been written in independent form. Applicants respectfully request that all claim changes and additions be entered at this time.

Claims 1-8, 12, 16, 18-20 and 23-24 were rejected under 35 U.S.C. 102(a) as being anticipated by Vuong et al. US patent application 2004/0017574 ("Vuong") for the reasons set forth on pages 2-5 of the action.

The present application relates to a method for adjusting the thickness of a thin semiconductor layer during a fabrication process. The method includes measuring the thickness of the layer, comparing this thickness to a standard profile that is stored in association with respective thickness adjustment specifications, selecting a stored standard profile to associate the layer with the respective thickness adjustment specification; and finally adjusting the thickness of the layer in accordance with the thickness adjustment specification. By measuring the thickness of the layer and comparing it to standard profiles, a surface treatment can be selected for adjusting the thickness of the layer to the desired thickness.

In contrast, Vuong discloses a method providing structure profiles which are compared to prior termination criteria and selection criteria. The analysis of the different parameters is realized to determinate if the termination criteria are met, and then, the selection criteria or the profile model are adjusted in consequence. In particular, a profile model for use in optical metrology of structures in a wafer is selected, where the profile model includes a set of geometric parameters associated with the dimensions of the structure. A set of optimization parameters is selected for the profile model using one or more input diffraction signals and one or more parameter selection criteria. The selected profile model and the set of optimization parameters are tested against one or more termination criteria. The process of selecting a profile model, selecting a set of optimization parameters, and testing the selected profile model and set of optimization parameters is performed until the one or more termination criteria are met.

There is no teaching or disclosure in Vuong to modify the thickness or surface profile of the layer, but instead Vuong describes a method to adjust the profile model defined by pre-determined criteria to the structure analyzed by diffraction signals (see Fig.2 ; P.2, §38). This method is aimed to the creation of a library of simulated diffraction signals and structure profiles, the display of results, profiles and parameter selection, or the use of results of profile and parameter selections for fabrication cluster loop controls. Indeed, the model profile of Vuong's process is directly defined after the characterization of the wafer structure (see p.3, §46) with possible optimization taking in count the selection criteria (p.3, §48), before the test with the predetermined criteria (p.3, §50).

The present invention is patentably distinct from Vuong because the profile models are already stored and the measures realized on the surface layer are compared to the stored profile model parameters to determine which one applies. He selected parameters then are used to adjust the thickness of the layer so that it conforms to the desired final thickness. The present invention does not make any adjustment of the model equipment parameters nor adjustment of the selection criteria as is performed in the process of Vuong. (see p.8 §90).

Although the same term, adjustment, is used in Vuong and in the present invention, the adjustment that is made in the present invention is directed towards the wafer structure that is submitted to this analysis, while in Vuong, at best, a measured profile is compared to known profiles to determine what it is. Thus, the goal of the present invention is to provide a method for adjusting the thickness of a semiconductor layer in accordance with the thickness adjustment specification in association with the model profile to meet certain product requirements, whereas in Vuong, comparisons are made for classification purposes but no modification of the wafer structure is suggested or made. Accordingly, the present claims are novel over the disclosure of Vuong and the anticipation rejection should be withdrawn.

Claims 9-11, 13-15 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Vuong in view of US patent 6,751,343 to Ferrell and Chapter 7 of the Wolf text entitled Silicon Processing for VLSI. The Examiner's reasons in support of this rejection appear on pages 5-7 of the office action.

Applicants repeat the comments made above regarding the Vuong reference. Ferrell discloses a method for indexing and retrieving manufacturing-

specific digital images based on image content. In a first step, at least one feature vector can be extracted from a manufacturing-specific digital image stored in an image database. In particular, each extracted feature vector corresponds to a particular characteristic of the manufacturing-specific digital image, for instance, a digital image modality and overall characteristic, a substrate/background characteristic, and an anomaly/defect characteristic. Notably, the extracting step includes generating a defect mask using a detection process. A second step includes using an unsupervised clustering method, with each extracted feature vector can be indexed in a hierarchical search tree. In a third step, a manufacturing-specific digital image associated with a feature vector stored in the hierarchicial search tree can be retrieved, wherein the manufacturing-specific digital image has image content comparably related to the image content of the query image. More particularly, can include two data reductions, the first performed based upon a query vector extracted from a query image. Subsequently, a user can select relevant images resulting from the first data reduction. From the selection, a prototype vector can be calculated, from which a second-level data reduction can be performed. The second-level data reduction can result in a subset of feature vectors comparable to the prototype vector, and further comparable to the query vector. An additional fourth step can include managing the hierarchical search tree by substituting a vector average for several redundant feature vectors encapsulated by nodes in the hierarchical search tree.

Like Vuong, Ferrell does not teach or disclose to use measured surface characteristics and to compare them to stored profiles to determine how to adjust the thickness of the surface to obtain a desired configuration. Ferrell discloses a method to extract one or more features of digital images from semiconductors, and then recording and indexing them to find the most similar images stored in the database of digital imagery. The method presents a method for fast retrieval (see col.2, line52) rather than for adjusting thickness or other surface parameters as in the present invention despite that the possibility of corrective action is mentioned at col.2, line 44.

The Wolf reference is also cited to supply additional information that is missing from Vuong and/or Ferrell. Wolf simply shows the formation of a SiO2 layer on Si by oxidation of Si to form the oxide. He also explains that the oxide thickness has to be measured (p.235, line 2) and that different techniques, such as optical interference, ellipsometry, capacitance, and color charts, are available for this purpose (p.235, lines 4-6). Like Vuong and Ferrell, however, Wolf does not disclose

techniques for adjusting the SiO2 layer by comparing the measured surface to a known profile so that adjustment parameters can be selected to adjust the thickness of the wafer to conform to the desired final thickness. Accordingly, the obviousness rejection of claim 1 has been overcome and should be withdrawn.

The dependent claims recite additional features of the invention. In particular, claim 16 recites that the thickness of the layer is adjusted simultaneously, as well as locally on different points of the wafer surface, while claim 18 recites treating batches of layers, wherein one layer thickness in the batch is adjusted by a certain given pitch while a subsequent layer thickness is being measured. These features are not mentioned at all in any of the cited references and the invention defined by that claim is further distinguishable from the references for that reason.

In view of the above, the entire application is believed to be in condition for allowance, early notice of which would be appreciated. Should any issues remain, a personal or telephonic interview is respectfully requested to discuss the same in order to expedite the allowance of all the claims in this application.

Respectfully submitted,

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